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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,186	DEWITT ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-7 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "interrupt unit control mechanism," "interrupt unit," and "performance monitoring unit" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed

invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the language "responsive ... control register" (lines 11-12) lack clear support from the specification. See also the 35 USC 112, 2nd paragraph above.

Claim Rejections - 35 USC § 101

Claims 16 and 23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

With regard to claims 16 and 23, as disclosed in the specification, the computer readable medium can be an "digital and analog communication links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions." It is clear that "radio frequency and light wave transmissions" may transmit but simply cannot store and record any instruction; and are not a tangible media.

Claim Rejections - 35 USC § 102

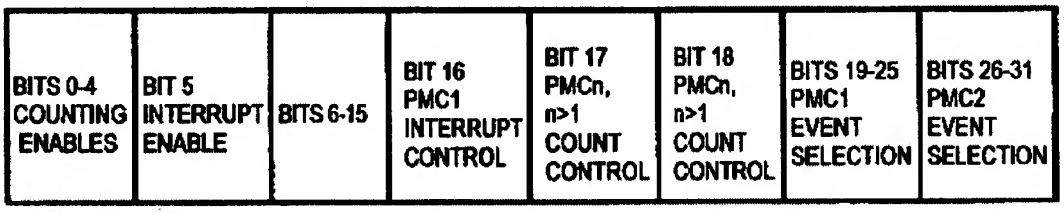
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-12, and 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Levine et al. (U.S. Patent No. 5,691,920).

Referring to claim 1: Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance-monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific

addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine disclosed two separate counters for selected events (figure 6A, column 8, lines 57-60). It is also clear that in Levine, at least bits 5 and 16 in a register field of a particular MMCR associated with a particular counter PMC indicate "an interrupt of a selected type" or specifically, the performance monitoring interrupt type. In other words, the type of interrupt indicated and associated with MMCR shown below is the performance monitoring interrupt type.



MONITOR MODE CONTROL REGISTER 0 (MMCR0)

FIGURE 6A

Further, it is also clear the performance monitoring interrupt is presented to the interrupt resolution logic or interrupt handler 57, which uses a plurality of interrupt handling routines to serve the interrupts depending from the types of interrupts. In other words, depending on a particular type of interrupt, the interrupt handler 57 will select a particular interrupt handling routine among the plurality of interrupt handling routines employed by the interrupt handler 57. It is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the

corresponding interrupt handling routine accordingly. In the instant case, the interrupt handler 57 must be able to determine that the presented interrupt is the performance monitoring interrupt before it selects a routine designed for performance monitoring. Thus, it is clear that the interrupt resolution logic or interrupt handler 57 is readable as the "interrupt unit."

Referring to claims 2-3: Since the nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine; thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 4: Levine discloses monitoring instruction execution and storage control (column 1, lines 65), which are the claimed multiple types of events.

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claims 8-10: It is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during servicing or processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance monitor unit 50. The counters count the

occurrence of events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

Referring to claim 11: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; furthermore, Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Since Levine discloses that it is preferred to examine all stages, Levine discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt.

Referring to claim 17: The nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine.

Referring to claim 18: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6, 8-14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Levine.

Referring to claim 1: The admitted prior art discloses a performance-monitoring unit (Specification, page 3, last paragraph, line 6) and one or more hardware counters (Specification, page 3, last paragraph, lines 1-2) located within the performance-monitoring unit. The admitted prior art does not disclose that the one or more hardware counters count the occurrence of events during an interrupt of a selected type.

Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-39); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck.

Referring to claim 2: Since an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and

interrupt service routine (Specification, page 4, 2nd paragraph, lines 3-11); thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 3: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 4: The admitted prior art discloses monitoring multiple types of events (Specification, page 3, last paragraph, lines 3-4, page 4, 1st paragraph, lines 5-7).

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claims 8-9: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt. However, in Levine, it is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during servicing or processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance

monitor unit 50. The counters count the occurrence of events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 10: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 11: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of

the interrupt or each state of the interrupt. Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Levine's examination on all stages are the claimed counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine teaches one on how to locate the performance bottleneck by tracing the processing through all stages.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 17: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 18: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or

more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Levine in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano.

Referring to claims 7, 15, and 22: The disclosures of the admitted prior art and Levine are stated above. As stated above, Levine discloses monitoring the particular interrupt according to the instructions address, and Levine discloses two separate counters for event selections (figure 6A, column 8, lines 57-60); thus, Levine discloses the hardware counters counting events separately. But neither explicitly discloses a second interrupt interrupts a first interrupt.

Mano discloses managing interrupt according to its priority (pages 434-435). Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

Response to Arguments

Applicants' arguments filed 11/01/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112, 2nd paragraph Rejection:

Applicants' amendment partially overcomes the 112, 2nd paragraph Rejection. In claims 1-7, the structural cooperative relationships between elements in the claims still have not been set forth. It is suggested that the word "coupled" (for example) be provided to overcome the rejection.

The 112, 1st paragraph Rejection:

In response to Applicants, while the Examiner agrees with Applicants that the specification, page 21, lines 26-28; and page 25, lines 18-20 provide support for the language, "an interrupt unit control register for indicating an interrupt type selected to be monitored, the Examiner disagrees with Applicants that the specification, page 21, lines 26-28; and page 25, lines 18-20 provide support for the language "an interrupt unit, in responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register."

The 101 Rejection:

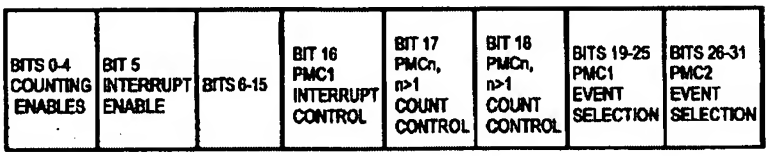
Applicants' amendment to the claims partially overcome the 101 Rejection. See the 101 Rejection above for details.

The 102 Rejection:

With regard to claims 1-6 and 23, Applicants argued that:

> Initially, Levine does not disclose or in any way suggest "an interrupt unit control register for indicating an interrupt type selected to be monitored" as presently recited in claim 1. Levine does not describe interrupt types and does not disclose a register that indicates an interrupt type selected to be monitored. Bits 5 and 16 illustrated in Figure 6A of Levine reproduced by the Examiner are not interrupt types selected to be monitored, but, at best, may relate to states of an interrupt.

Contrary to Applicants' argument, it is clear from Fig. 6A below that shows a register:



MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

wherein at least bits 5 and 16 in a register field of a particular MMCR associated with a particular counter PMC indicate "an interrupt of a selected type" or specifically, the performance monitoring interrupt type. In other words, the type of interrupt indicated and associated with MMCR shown below is the performance monitoring interrupt type. It is noted that Applicants have not provided any reason or explanation to support Applicants' assertion that bits 6 and 16 do not indicate the type of interrupt selected.

Applicants also argued that:

> Furthermore, Levine does not disclose "an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as now recited in claim 1. In rejecting the claims, the Examiner construes the interrupt handler 57 in Levine as corresponding to the interrupt unit recited in claim 1. In particular, the Examiner points out that interrupt handler 57 in Levine selects one of interrupt handling routines 71, 77 and 79 illustrated in Figure 4, and concludes "[i]t is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly." Applicants respectfully disagree.
>
> Applicants respectfully submit that Levine nowhere discloses or suggests that interrupt handler 57 selects one or another of interrupt handling routines 71, 77 and 79 based on interrupt type, and Levine certainly does not disclose that interrupt handler 57 selects a particular interrupt handling routine based on an interrupt type selected to be monitored. Neither the Monitor Mode Control Register illustrated in Figure 6A referred to by the Examiner nor the discussion of the interrupt handling routines in column 9, lines 46-62 in Levine suggests that interrupt handler 57 selects a particular interrupt routine based on interrupt type. Levine does not disclose that interrupt handler 57 functions to be "responsive to an interrupt occurring during code execution for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as now recited in claim 1.

Contrary to Applicants' argument, as acknowledged by Applicants, "the interrupt handler 57 selects a particular interrupt handling routine based on the interrupt type." As discussed above, in the register fields of the register shown in Fig. 6A below:

BITS 0-4 COUNTING ENABLES	BIT 5 INTERRUPT ENABLE	BITS 6-15	BIT 16 PMC1 INTERRUPT CONTROL	BIT 17 PMCn, n>1 COUNT CONTROL	BIT 18 PMCn, n>1 COUNT CONTROL	BITS 19-25 PMC1 EVENT SELECTION	BITS 26-31 PMC2 EVENT SELECTION

MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

As disclosed by Levine, the MMCR0 is partitioned into a number of bit fields whose settings select events to be counted, enable performance

monitor interrupts, specify the conditions under which counting is enabled, and set a threshold value (X) (emphasis added). Thus, it is clear that at least bit 5 needs to be set to enable generation of a particular type of interrupt such as the performance monitor interrupt. Responsive to the set bit 5, a particular type of interrupt such as a performance monitor interrupt is provided to the interrupt handler 47, which would select a particular interrupt routine based on the interrupt type.

Applicants also argued that:

> Levine also does not disclose or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register." Although Levine may disclose counters in performance monitor 50 illustrated in Figure 4 of Levine, the counters are described as being for counting "processor/storage related events" (see col. 8, lines 33-41 of Levine). Levine does not disclose that the counters count events that occur during processing of an interrupt "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as required in claim 1. Levine does not disclose interrupt types and does not determine if an interrupt that occurs during code execution is of an interrupt type selected to be monitored.

Contrary to Applicants' argument, Levine, as a matter of fact, discloses one or more hardware counter located within the performance monitoring unit. As clearly shown in Fig. 4, which is reproduced below;

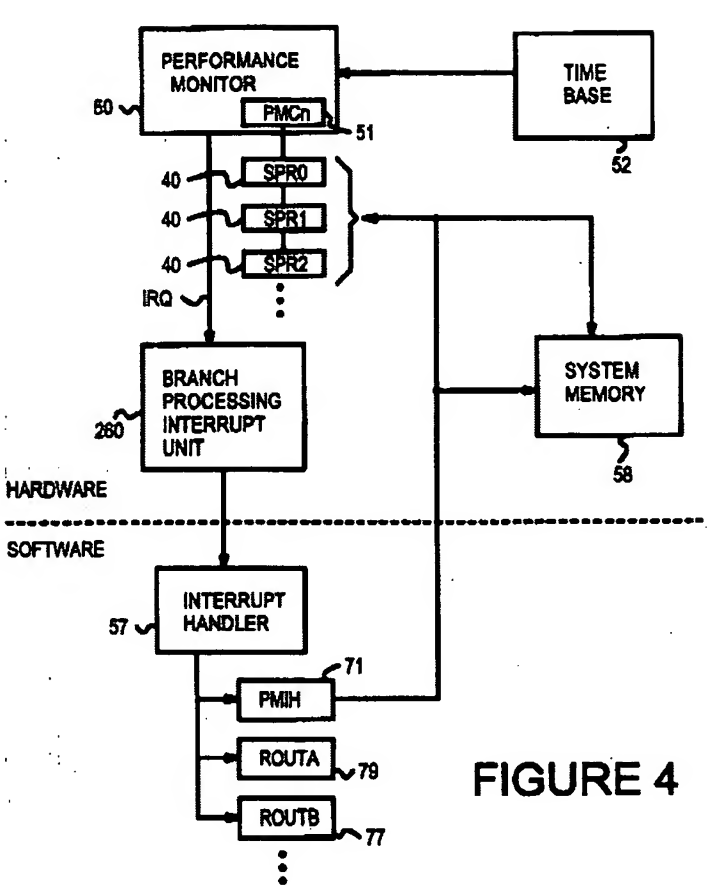
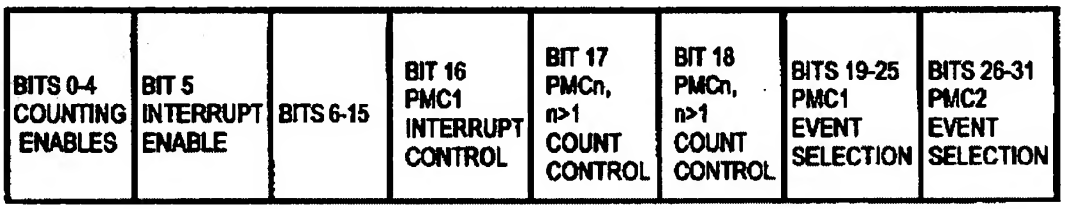


FIGURE 4

one or more hardware counters PMCn 51 are located within the performance monitor 50. As also disclosed by Levine, the performance monitor 50 is intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes counters 51 for counting processor/storage related events. See at least column 8, lines 33-41. Levine further discloses that when the performance monitor 50 receives the notification from time base 52 to indicate that it should record "sample data", an interrupt signal is output to a branch processing unit 20. Such interrupt type is called "a performance monitoring interrupt" occurred at a selectable point in the processing. As in any type of interrupt, the performance monitor interrupt causes the processor to save its

state of execution, and begin execution of an interrupt handler (also known as interrupt service routine). It is clear that in this case, during servicing or processing the performance mnitor interrupt, the service routine for the performance monitring interrupt monitors performance by counting the number of related events. See at least column 9, line 63 to column 10, line 32. In addition, it is clear that in Levine, at least bits 5 and 16 in a register field of a particular MMCR associated with a particular counter PMC indicate "an interrupt of a selected type" or specifically, the performance monitoring interrupt type. In other words, the type of interrupt indicated and associated with MMCR shown below is the performance monitoring interrupt type.



MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

As disclosed by Levine, the MMCR0 is partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, specify the conditions under which counting is enabled, and set a threshold value (X) (emphasis added). Thus, it is clear that at least bit 5 needs to be set to enable generation of a particular type of interrupt such as the performance monitor interrupt. Responsive to the set bit 5, a particular type of interrupt such as a

performance monitor interrupt is provided to the interrupt handler 47, which would select a particular interrupt routine based on the interrupt type.

Further, it is also clear the performance monitoring interrupt is presented to the interrupt resolution logic or interrupt handler 57, which uses a plurality of interrupt handling routines to serve the interrupts depending from the types of interrupts. In other words, depending on a particular type of interrupt, the interrupt handler 57 will select a particular interrupt handling routine among the plurality of interrupt handling routines employed by the interrupt handler 57. It is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly. In the instant case, the interrupt handler 57 must be able to determine that the presented interrupt is the performance monitoring interrupt before it selects a routine designed for performance monitoring. Thus, it is clear that the interrupt resolution logic or interrupt handler 57 is readable as the "interrupt unit."

In response to Applicants' argument regarding claims 8 and 16, see discussion above. Further, it is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during servicing or processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance monitor unit 50. The counters count the occurrence of events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

The 103 Rejection:

With regard to claims 1-6, 8-14, and 16-21, Applicants argued that:

> In the present case, neither the admitted prior art nor Levine nor their combination discloses or suggests "an interrupt unit control register for indicating an interrupt type selected to be monitored", "an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register", or "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register" as recited in claim 1. Levine does not disclose the subject matter of claim 1 for reasons discussed in detail above. The admitted prior art is cited as disclosing a performance monitoring unit having hardware counters, and does not supply the deficiencies in Levine. Accordingly, the references do not teach all of the features of the claimed invention as recited in claim 1, and the Examiner has, thus, not established a *prima facie* case of obviousness in rejecting claim 1.
>
> For similar reasons as discussed above, the admitted prior art in view of Levine also does not teach all of the features of the claimed invention as recited in claims 8 and 16, and the Examiner has also not established a *prima facie* case of obviousness in rejecting claims 8 and 16 as well.

In response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). As discussed above, the acknowledged

prior art discloses "one or more hardware counter located within the performance monitoring unit." Levine, in Fig. 4, which is reproduced below;

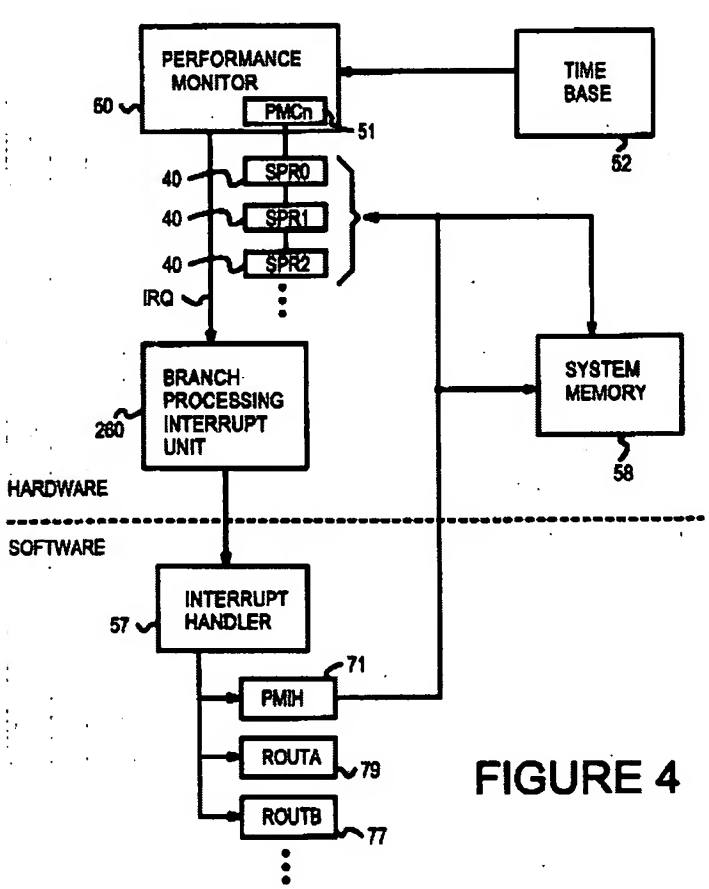


FIGURE 4

discloses one or more hardware counters PMCn 51 are located within the performance monitor 50. As also disclosed by Levine, the performance monitor 50 is intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes counters 51 for counting processor/storage related events. See at least column 8, lines 33-41. Levine further discloses that when the performance monitor 50 receives the notification from time base 52 to indicate that it should record "sample data", an interrupt signal is output to a branch processing unit 20. Such interrupt type is

called "a performance monitoring interrupt" occurred at a selectable point in the processing. As in any type of interrupt, the performance monitor interrupt causes the processor to save its state of execution, and begin execution of an interrupt handler (also known as interrupt service routine). It is clear that in this case, during servicing or processing the performance mnitor interrupt, the service routine for the performance monitring interrupt monitors performance by counting the number of related events. See at least column 9, line 63 to column 10, line 32. In addition, it is clear that in Levine, at least bits 5 and 16 in a register field of a particular MMCR associated with a particular counter PMC indicate "an interrupt of a selected type" or specifically, the performance monitoring interrupt type. In other words, the type of interrupt indicated and associated with MMCR shown below is the performance monitoring interrupt type.

BITS 0-4 COUNTING ENABLES	BIT 5 INTERRUPT ENABLE	BITS 6-15	BIT 16 PMC1 INTERRUPT CONTROL	BIT 17 PMCn, n>1 COUNT CONTROL	BIT 18 PMCn, n>1 COUNT CONTROL	BITS 19-25 PMC1 EVENT SELECTION	BITS 26-31 PMC2 EVENT SELECTION

MONITOR MODE CONTROL REGISTER 0
(MMCR0)

FIGURE 6A

As disclosed by Levine, the MMCR0 is partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, specify the conditions under which counting is enabled, and set a threshold value (X) (emphasis added). Thus, it is clear that at least bit 5 needs to be set to enable generation of a particular type of interrupt such as the performance

monitor interrupt. Responsive to the set bit 5, a particular type of interrupt such as a performance monitor interrupt is provided to the interrupt handler 47, which would select a particular interrupt routine based on the interrupt type.

Further, it is also clear the performance monitoring interrupt is presented to the interrupt resolution logic or interrupt handler 57, which uses a plurality of interrupt handling routines to serve the interrupts depending from the types of interrupts. In other words, depending on a particular type of interrupt, the interrupt handler 57 will select a particular interrupt handling routine among the plurality of interrupt handling routines employed by the interrupt handler 57. It is clear that the interrupt handler 57 MUST be able to determine which type of interrupt presented to it before it selects the corresponding interrupt handling routine accordingly. In the instant case, the interrupt handler 57 must be able to determine that the presented interrupt is the performance monitoring interrupt before it selects a routine designed for performance monitoring. Thus, it is clear that the interrupt resolution logic or interrupt handler 57 is readable as the "interrupt unit."

Further, as clearly stated in the 103 Rejection, the benefits and advantages are readily realized by employing the performance monitor taught by Levine. As set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage

or expected beneficial result, which would have been produced by the combination, is a significant improvement in system performance, obtained by indicating and resolving performance bottlenecks.

With regard to claims 7, 15, and 22, Applicants argued that:

> In addition, although Mano may disclose monitoring interrupts according to their priority, the reference does not disclose or suggest "a second interrupt that interrupts the first interrupt, wherein the one or more hardware counters separately count the events that occur during the processing of the first interrupt and events that occur during processing of the second interrupt" as more clearly recited in amended claim 7 and corresponding claims 15 and 22. As pointed out above, although Levine may disclose counters in performance monitor 50 illustrated in Figure 4 of Levine, the counters are described as being for counting "processor/storage related events", and Levine also does not disclose hardware counters that separately count events that occur during the processing of the first interrupt and events that occur during processing of the second interrupt" as recited in claims 7, 15 and 22. Accordingly, claims 7, 15 and 22 are also allowable in their own right as well as by virtue of their dependency.

In response to Applicants' argument, Applicants cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As clearly discussed above, in Levine, multiples events are counted separately by hardware counters during servicing or processing of a performance monitor interrupt. Further, the performance monitor interrupt is occurred at a selectable point in the processing. Depending on the number of "sample data" requests, multiple performance monitor interrupts can be generated, and events are separately counted during servicing or processing of a respective performance monitor interrupt.

Further, by definition, an interrupt (second interrupt, for example) interrupts another interrupt process (first interrupt, for example). See definition of Interrupt by Wikipedia, cited IN Form-892. In any event, Mano discloses managing interrupt according to its priority (pages 434-435). Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner